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L4	255	(SIMD SISD) with (status state$3)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/02/06 14:04
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L8	276	6 and @ad<"20010322"	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/02/06 14:06
L9	116	(712/30).CCLS.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/02/06 14:06

L10	0	7 and 9	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/02/06 14:06
L11	2	8 and 9	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/02/06 14:06
L12	2	("20020156993").PN.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/02/06 14:07
S1	2	("20020156993").PN.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/02/06 14:07
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S6	0	(SIMD SISD) with (DRAM) with (status)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/02/06 14:04
S7	1534	((plural$5 multiple$3) adj3 processor$5) and (simd sisd mimd)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/02/06 14:04
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S9	25	S8 and @ad<"20010322"	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/02/06 14:05
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1 A distributed shared memory multiprocessor ASURA: memory and cache architecture

S. Mori, H. Saito, M. Goshima, S. Tomita, M. Yanagihara, T. Tanaka, D. Fraser, K. Joe, H. Nitta

December 1993 **Proceedings of the 1993 ACM/IEEE conference on Supercomputing**

Publisher: ACM Press

Full text available: pdf(1.17 MB) Additional Information: full citation, references, citings, index terms

2 Decoupled hardware support for distributed shared memory

Steven K. Reinhardt, Robert W. Pfile, David A. Wood

May 1996 **ACM SIGARCH Computer Architecture News , Proceedings of the 23rd annual international symposium on Computer architecture ISCA '96**, Volume 24 Issue 2

Publisher: ACM Press

Full text available: pdf(1.47 MB) Additional Information: full citation, abstract, references, citings, index terms

This paper investigates hardware support for fine-grain distributed shared memory (DSM) in networks of workstations. To reduce design time and implementation cost relative to dedicated DSM systems, we decouple the functional hardware components of DSM support, allowing greater use of off-the-shelf devices.We present two decoupled systems, Typhoon-0 and Typhoon-1. Typhoon-0 uses an off-the-shelf protocol processor and network interface; a custom access control device is the only DSM-specific hard ...

3 Efficient synchronization primitives for large-scale cache-coherent multiprocessors

James R. Goodman, Mary K. Vernon, Philip J. Woest

April 1989 **ACM SIGARCH Computer Architecture News , Proceedings of the third international conference on Architectural support for programming languages and operating systems ASPLOS-III**, Volume 17 Issue 2

Publisher: ACM Press

Full text available: pdf(1.48 MB) Additional Information: full citation, abstract, references, citings, index terms

This paper proposes a set of efficient primitives for process synchronization in multiprocessors. The only assumptions made in developing the set of primitives are that hardware combining is not implemented in the inter-connect, and (in one case) that the interconnect supports broadcast. The primitives make use of synchronization bits (syncbits) to provide a simple mechanism for mutual exclusion. The proposed implementation of the primitives includes efficient (i.e.

4

Flexible use of memory for replication/migration in cache-coherent DSM multiprocessors

Vijayaraghavan Soundararajan, Mark Heinrich, Ben Verghese, Kourosh Gharachorloo, Anoop Gupta, John Hennessy

April 1998 **ACM SIGARCH Computer Architecture News , Proceedings of the 25th annual international symposium on Computer architecture ISCA '98**, Volume 26 Issue 3

Publisher: IEEE Computer Society, ACM Press

Full text available: pdf(1.76 MB) Additional Information: full citation, abstract, references, citings, index terms

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Given the limitations of bus-based multiprocessors, CC-NUMA is the scalable architecture of choice for shared-memory machines. The most important characteristic of the CC-NUMA architecture is that the latency to access data on a remote node is considerably larger than the latency to access local memory. On such machines, good data locality can reduce memory stall time and is therefore a critical factor in application performance.In this paper we study the various options available to system desi ...

5 Efficient management of memory hierarchies in embedded DRAM systems

Ashley Saulsbury, Su-Jaen Huang, Fredrik Dahlgren

May 1999 **Proceedings of the 13th international conference on Supercomputing**

Publisher: ACM Press

Full text available: pdf(1.57 MB) Additional Information: full citation, references, index terms

Keywords: COMA, DRAM, cache, latency, memory hierarchy, processor

6 Analytic evaluation of shared-memory systems with ILP processors

Daniel J. Sorin, Vijay S. Pai, Sarita V. Adve, Mary K. Vernon, David A. Wood

April 1998 **ACM SIGARCH Computer Architecture News , Proceedings of the 25th annual international symposium on Computer architecture ISCA '98**, Volume 26 Issue 3

Publisher: IEEE Computer Society, ACM Press

Full text available: pdf(1.45 MB) Additional Information: full citation, abstract, references, citings, index terms

Publisher Site

This paper develops and validates an analytical model for evaluating various types of architectural alternatives for shared-memory systems with processors that aggressively exploit instruction-level parallelism. Compared to simulation, the analytical model is many orders of magnitude faster to solve, yielding highly accurate system performance estimates in seconds.The model input parameters characterize the ability of an application to exploit instruction-level parallelism as well as the interac ...

7 The Stanford FLASH multiprocessor

Jeffrey Kuskin, David Ofelt, Mark Heinrich, John Heinlein, Richard Simoni, K. Gharachorloo, J. Chapin, D. Nakahira, J. Baxter, M. Horowitz, A. Gupta, M. Rosenblum, J. Hennessy

August 1998 **25 years of the international symposia on Computer architecture (selected papers)**

Publisher: ACM Press

Full text available: pdf(1.48 MB) Additional Information: full citation, references, index terms

8 The M-Machine multicomputer

Marco Fillo, Stephen W. Keckler, William J. Dally, Nicholas P. Carter, Andrew Chang, Yevgeny Gurevich, Whay S. Lee

December 1995 **Proceedings of the 28th annual international symposium on Microarchitecture**

Publisher: IEEE Computer Society Press
Full text available: pdf(1.29 MB) Additional Information: full citation, references, citings, index terms

9 The directory-based cache coherence protocol for the DASH multiprocessor
Daniel Lenoski, James Laudon, Kourosh Gharachorloo, Anoop Gupta, John Hennessy
May 1990 **ACM SIGARCH Computer Architecture News , Proceedings of the 17th annual international symposium on Computer Architecture ISCA '90**, Volume 18 Issue 3a
Publisher: ACM Press
Full text available: pdf(1.74 MB) Additional Information: full citation, abstract, references, citings, index terms

DASH is a scalable shared-memory multiprocessor currently being developed at Stanford's Computer Systems Laboratory. The architecture consists of powerful processing nodes, each with a portion of the shared-memory, connected to a scalable interconnection network. A key feature of DASH is its distributed directory-based cache coherence protocol. Unlike traditional snoopy coherence protocols, the DASH protocol does not rely on broadcast; instead it uses point-to-point messages sent between th ...

10 A survey of commercial parallel processors
Edward Gehringer, Janne Abullarade, Michael H. Gulyn
September 1988 **ACM SIGARCH Computer Architecture News**, Volume 16 Issue 4
Publisher: ACM Press
Full text available: pdf(2.96 MB) Additional Information: full citation, abstract, citings, index terms

This paper compares eight commercial parallel processors along several dimensions. The processors include four shared-bus multiprocessors (the Encore Multimax, the Sequent Balance system, the Alliant FX series, and the ELXSI System 6400) and four network multiprocessors (the BBN Butterfly, the NCUBE, the Intel iPSC/2, and the FPS T Series). The paper contrasts the computers from the standpoint of interconnection structures, memory configurations, and interprocessor communication. Also, the share ...

11 Evaluation of design alternatives for a multiprocessor microprocessor
Basem A. Nayfeh, Lance Hammond, Kunle Olukotun
May 1996 **ACM SIGARCH Computer Architecture News , Proceedings of the 23rd annual international symposium on Computer architecture ISCA '96**, Volume 24 Issue 2
Publisher: ACM Press
Full text available: pdf(1.37 MB) Additional Information: full citation, abstract, references, citings, index terms

In the future, advanced integrated circuit processing and packaging technology will allow for several design options for multiprocessor microprocessors. In this paper we consider three architectures: shared-primary cache, shared-secondary cache, and shared-memory. We evaluate these three architectures using a complete system simulation environment which models the CPU, memory hierarchy and I/O devices in sufficient detail to boot and run a commercial operating system. Within our simulation envir ...

12 CRL: high-performance all-software distributed shared memory
K. L. Johnson, M. F. Kaashoek, D. A. Wallach
December 1995 **ACM SIGOPS Operating Systems Review , Proceedings of the fifteenth ACM symposium on Operating systems principles SOSP '95**, Volume 29 Issue 5
Publisher: ACM Press
Full text available: pdf(2.02 MB) Additional Information: full citation, references, citings, index terms

13 Coherent network interfaces for fine-grain communication
Shubhendu S. Mukherjee, Babak Falsafi, Mark D. Hill, David A. Wood

May 1996 **ACM SIGARCH Computer Architecture News , Proceedings of the 23rd annual international symposium on Computer architecture ISCA '96**, Volume 24 Issue 2

Publisher: ACM Press

Full text available: pdf(1.72 MB) Additional Information: full citation, abstract, references, citings, index terms

Historically, processor accesses to memory-mapped device registers have been marked uncachable to insure their visibility to the device. The ubiquity of snooping cache coherence, however, makes it possible for processors and devices to interact with cachable, coherent memory operations. Using coherence can improve performance by facilitating burst transfers of whole cache blocks and reducing control overheads (e.g., for polling).This paper begins an exploration of network interfaces (NIs) that u ...

14 Where is time spent in message-passing and shared-memory programs?

Satish Chandra, James R. Larus, Anne Rogers

November 1994 **ACM SIGPLAN Notices , ACM SIGOPS Operating Systems Review , Proceedings of the sixth international conference on Architectural support for programming languages and operating systems ASPLOS-VI**, Volume 29 , 28 Issue 11 , 5

Publisher: ACM Press

Full text available: pdf(1.55 MB) Additional Information: full citation, abstract, references, citings, index terms

Message passing and shared memory are two techniques parallel programs use for coordination and communication. This paper studies the strengths and weaknesses of these two mechanisms by comparing equivalent, well-written message-passing and shared-memory programs running on similar hardware. To ensure that our measurements are comparable, we produced two carefully tuned versions of each program and measured them on closely-related simulators of a message-passing and a shared-memory machine, ...

15 Synchronization and communication in the T3E multiprocessor

Steven L. Scott

September 1996 **ACM SIGPLAN Notices , ACM SIGOPS Operating Systems Review , Proceedings of the seventh international conference on Architectural support for programming languages and operating systems ASPLOS-VII**, Volume 31 , 30 Issue 9 , 5

Publisher: ACM Press

Full text available: pdf(1.34 MB) Additional Information: full citation, abstract, references, citings, index terms

This paper describes the synchronization and communication primitives of the Cray T3E multiprocessor, a shared memory system scalable to 2048 processors. We discuss what we have learned from the T3D project (the predecessor to the T3E) and the rationale behind changes made for the T3E. We include performance measurements for various aspects of communication and synchronization.The T3E augments the memory interface of the DEC 21164 microprocessor with a large set of explicitly-managed, external r ...

16 Tempest and typhoon: user-level shared memory

S. K. Reinhardt, J. R. Larus, D. A. Wood

April 1994 **ACM SIGARCH Computer Architecture News , Proceedings of the 21ST annual international symposium on Computer architecture ISCA '94**, Volume 22 Issue 2

Publisher: IEEE Computer Society Press, ACM Press

Full text available: pdf(1.44 MB) Additional Information: full citation, abstract, references, citings, index terms

Future parallel computers must efficiently execute not only hand-coded applications but also programs written in high-level, parallel programming languages. Today's machines limit these programs to a single communication paradigm, either message-passing or shared-memory, which results in uneven performance. This paper addresses this problem by defining an interface, *Tempest*, that exposes low-level communication and memory-

system mechanisms so programmers and compilers can customize polici ...

17 The design of RPM: an FPGA-based multiprocessor emulator

Koray Öner, Luiz A. Barroso, Sasan Iman, Jaeheon Jeong, Krishnan Ramamurthy, Michel Dubois

February 1995 **Proceedings of the 1995 ACM third international symposium on Field-programmable gate arrays**

Publisher: ACM Press

Full text available: pdf(54.01 KB) Additional Information: full citation, abstract, references, citings, index terms

Recent advances in Field-Programmable Gate Arrays (FPGA) and programmable interconnects have made it possible to build efficient hardware emulation engines. In addition, improvements in Computer-Aided Design (CAD) tools, mainly in synthesis tools, greatly simplify the design of large circuits. The RPM (Rapid Prototype Engine for Multiprocessors) Project leverages these two technological advances. Its goal is to develop a common hardware platform for th ...

Keywords: field-programmable gate arrays, logic emulation, message-passing multicomputers, rapid prototyping, shared-memory multiprocessors

18 The MIT Alewife machine: architecture and performance

Anant Agarwal, Ricardo Bianchini, David Chaiken, Kirk L. Johnson, David Kranz, John Kubiatowicz, Beng-Hong Lim, Kenneth Mackenzie, Donald Yeung

May 1995 **ACM SIGARCH Computer Architecture News , Proceedings of the 22nd annual international symposium on Computer architecture ISCA '95**, Volume 23 Issue 2

Publisher: ACM Press

Full text available: pdf(1.49 MB) Additional Information: full citation, abstract, references, citings, index terms

Alewife is a multiprocessor architecture that supports up to 512 processing nodes connected over a scalable and cost-effective mesh network at a constant cost per node. The MIT Alewife machine, a prototype implementation of the architecture, demonstrates that a parallel system can be both scalable and programmable. Four mechanisms combine to achieve these goals: software-extended coherent shared memory provides a global, linear address space; integrated message passing allows compiler and operat ...

19 OMP: a RISC-based multiprocessor using orthogonal-access memories and multiple spanning buses

K. Hwang, M. Dubois, D. K. Panda, S. Rao, S. Shang, A. Uresin, W. Mao, H. Nair, M. Lytwyn, F. Hsieh, J. Liu, S. Mehrotra, C. M. Cheng

June 1990 **ACM SIGARCH Computer Architecture News , Proceedings of the 4th international conference on Supercomputing ICS '90**, Volume 18 Issue 3b

Publisher: ACM Press

Full text available: pdf(1.96 MB) Additional Information: full citation, abstract, references, citings, index terms

This paper presents the architectural design and RISC based implementation of a prototype supercomputer, namely the Orthogonal MultiProcessor (OMP). The OMP system is constructed with 16 Intel 1860 RISC microprocessors and 256 parallel memory modules, which are 2-D interleaved and orthogonally accessed using custom-designed spanning buses. The architectural design has been validated by a CSIM-based multiprocessor simulator. The design choices are based on worst-case delay a ...

20 A programming model for the Mark III hypercube with multiple processor nodes

B. A. Zimmermann, G. A. Crichton

January 1988 **Proceedings of the third conference on Hypercube concurrent computers and applications: Architecture, software, computer systems, and general issues - Volume 1**

Publisher: ACM Press

Full text available: pdf(567.05 KB) Additional Information: full citation, abstract, references, index terms

The Caltech/JPL Mark III Hypercube originally consisted of an ensemble of processing elements each containing two Motorola M68020 processors — one M68020 processor and a M68881 Floating-Point coprocessor used for data processing, the other M68020 processor dedicated to hypercube communications. In the interest of achieving even greater computational capability a third processing element, the Weitek XL system, was added to enhance floating point performance. Each of what is now three p ...

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IEE CNF	IEE Conference Proceeding
IEEE STD	IEEE Standard

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1. **The Scalable Coherent Interface, IEEE P 1596, status and possible applications to data acquisition and physics**
Gustavson, D.B.;
Nuclear Science, IEEE Transactions on
Volume 37, Issue 2, Part 2, April 1990 Page(s):365 - 368
Digital Object Identifier 10.1109/23.106646
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2. **Fine grain scheduler for shared-memory multiprocessor systems**
Shieh, J.-J.; Lee, Y.-C.; Chen, H.-R.;
Computers and Digital Techniques, IEE Proceedings-
Volume 142, Issue 2, March 1995 Page(s):98 - 106
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3. **Multicomputers: message-passing concurrent computers**
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Volume 21, Issue 8, Aug. 1988 Page(s):9 - 24
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4. **IEEE P1596, a scalable coherent interface for gigabyte/sec multiprocessor applications**
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Nuclear Science, IEEE Transactions on
Volume 36, Issue 1, Part 1, Feb. 1989 Page(s):811 - 812
Digital Object Identifier 10.1109/23.34555
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5. **Dependability modeling for multiprocessors**
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Computer
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Gustavson, D.B.; Qiang Li;

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4-8 June 2005 Page(s):246 - 257
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Aerospace and Electronics Conference, 1997. NAECON 1997., Proceedings of the IEEE 1997 National
Volume 1, 14-17 July 1997 Page(s):378 - 385 vol.1
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Kuskin, J.; Ofelt, D.; Heinrich, M.; Heinlein, J.; Simoni, R.; Gharachorloo, K.; Chapin, J.; Nakahira, D.; Baxter, J.; Horowitz, M.; Gupta, A.; Rosenblum, M.; Hennessy, J.;
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